Claims

[c1] A method of forming a semiconductor structure comprising steps of:forming spacer voids between a gate a the mandrel layer;
creating recesses in a substrate below and in alignment with the spacer voids;
filling a first portion of recesses with a stress imposing material;
filling a second portion of the recesses with a semiconductor material; and
removing the mandrel layer.

[c2] A method according to claim 1, further including forming dummy spacers between the mandrel layer and the gate and forming a nitride interface as an etch stop in the recesses.

[c3] A method according to claim 1, wherein the recesses include a first recess and a second recess, the first recess and the second recess having a depth greater than a depth of the bottom of a channel area of the gate.

[c4] A method according to claim 3, wherein the first recess has a depth substantially equal to the depth of the sec-

ond recess.

[c5] A method according to claim 3, wherein the first recess has a depth of about 500 to 2000 angstroms.

[c6] A method according to claim 1, further comprising forming dummy spacers and removing the dummy spacers to form the spacer voids, wherein:
a first dummy spacer has a first width;
a second dummy spacer has a second width;
a first recess of the recesses has a width substantially equal to the first width of the first dummy spacer; and
a second recess of the recesses has a width substantially equal to the second width of the second dummy spacer.

[c7] A method according to claim 6, wherein the first width is substantially equal to the second width.

[c8] A method according to claim 7, wherein the first width is about 100 to 1000 Å.

[c9] A method according to claim 1, wherein the recesses are substantially equidistant from the gate.

[c10] A method according to claim 1, wherein the stress imposing material is a material that introduces a compressive stress.

[c11] A method according to claim 1, wherein the stress im-

posing material is a material that introduces a tensile stress.

[c12] A method according to claim 1, wherein the stress imposing material is a material that introduces a stress that degrades electron or hole mobility in the semiconductor structure.

[c13] A method according to claim 1, wherein the stress imposing material is a material that introduces a stress that enhances electron or hole mobility in the semiconductor structure.

[c14] A method according to claim 1, wherein the stress imposing material is a material comprised of at least one of polysilicon, $SiO_{2,}$ $Si_{1-x}Ge_x$, Si_xN_y, or Si_xON_y.

[c15] A method according to claim 1, wherein the semiconductor material is comprised of epitaxially grown Si.

[c16] A method according to claim 1, wherein:
the gate is an n-channel field effect transistor gate; and the stress imposing material is a material that introduces a tensile stress in a direction parallel to a direction of current flow for the n-channel field effect transistor gate.

[c17] A method according to claim 1, wherein:

the gate is a p-channel field effect transistor gate; and
the stress imposing material is a material that introduces a compressive stress in a direction parallel to a direction of current flow for the p-channel field effect transistor gate.

[c18] A method according to claim 1, further comprising a step of annealing after filling the first portion of the first recess and the first portion of the second recess with a stress imposing material.

[c19] A method of forming a semiconductor structure comprising steps of:
forming first dummy spacers on sides of a gate formed on a substrate;
forming a mandrel layer with portions of the mandrel layer abutting the dummy spacers;
removing the dummy spacers to form spacer voids between the gate and mandrel layer;
creating recesses in the substrate below and in alignment with the spacer void;
filling a first portion of the recesses with a stress imposing material; and
filling a second portion of the recesses with a semiconductor material.

[c20] A method according to claim 19, further comprising the

steps of:

filling a second portion of the recesses with a semiconductor material; and

removing the mandrel layer, wherein:

the first portion of the recesses is below the bottom of a channel area of the gate; and

the stress imposing material is a material that introduces one of a compressive stress and a tensile stress in the channel area.

[c21] A method according to claim 19, wherein the stress imposing material is a material comprised of at least one of polysilicon, $SiO_{2,}$ $Si_{1-x}Ge_x$, Si_xN_y, or Si_xON_y.

[c22] A method according to claim 20, wherein the gate is one of:

an n-channel field effect transistor gate and the stress imposing material is a material that introduces a tensile stress in a direction parallel to a direction of current flow for the n-channel field effect transistor gate; and

a p-channel field effect transistor gate and the stress imposing material is a material that introduces a compressive stress in a direction parallel to a direction of current flow for the p-channel field effect transistor gate.

[c23] A method of forming a semiconductor structure com-

prising steps of:
forming a first type of field effect transistor gate and a second type of field effect transistor gate on a substrate;
forming a first dummy spacer and a second dummy spacer on sides of the first type of field effect transistor gate and on sides of the second type of field effect transistor gate;
forming a mandrel layer with first portions of the mandrel layer abutting the first and second dummy spacers for the first type of field effect transistor gate and second portions of the mandrel layer abutting the first and second dummy spacers for the second type of field effect transistor gate;
masking the second type of field effect transistor gate and the first and second dummy spacers for the second type of field effect transistor gate and introducing stress material for the first type of field effect transistor gate;
masking the first type of field effect transistor gate and the first and second dummy spacers for the first type of field effect transistor gate and introducing stress material for the first type of field effect transistor gate; and
removing the mandrel layer;
wherein the step of introducing stress material is comprised of
removing the first and second dummy spacers from the unmasked field effect transistor gate to form first and

second spacer voids between the gate and first portions of the mandrel layer;

creating a first recess in the substrate below and in alignment with the first spacer void and a second recess in the substrate below and in alignment with the second spacer void for the unmasked field effect transistor gate;

filling a first portion of the first recess and a first portion of the second recess for the unmasked field effect transistor gate with a stress imposing material configured to enhance performance of the unmasked field effect transistor gate;

filling a second portion of the first recess and a second portion of the second recess for the unmasked field effect transistor gate with a semiconductor material; and

unmasking the masked field effect transistor gate and the first and second dummy spacers for the masked field effect transistor gate.

[c24] A method according to claim 23, wherein the steps are performed in the order recited.

[c25] A method according to claim 23, wherein:

the first type of field effect transistor gate is an n-channel field effect transistor gate and the stress imposing material configured to enhance performance of the n-channel field effect transistor gate is a material that introduces a tensile stress in a direction parallel to a di-

rection of current flow for the n-channel field effect transistor gate; and
the second type of field effect transistor gate is a p-channel field effect transistor gate and the stress imposing material configured to enhance performance of the p-channel field effect transistor gate is a material that introduces a compressive stress in a direction parallel to a direction of current flow for the n-channel field effect transistor gate.

[c26] A semiconductor structure, comprising:
a substrate;
a field effect transistor gate on the substrate, the gate having a first side and a second side;
a first spacer against a first side of the gate;
a second spacer against a second side of the gate;
a first recess in the substrate, the first recess being approximately directly below the first spacer and having a first side approximately in alignment with the first side of the gate;
a second recess in the substrate, the second recess being approximately directly below the second spacer and having a second side approximately in alignment with the second side of the gate;
a material imposing stress filling a first portion of the first recess and a first portion of the second recess;

a semiconductor material filling a second portion of the first recess and a second portion of the second recess.

[c27] A semiconductor structure according to claim 26, wherein the stress imposing material is a material that introduces one of a compressive stress and a tensile stress.

[c28] A semiconductor structure according to claim 26, wherein the stress imposing material is a material comprised of at least one of polysilicon, $SiO_{2,}$ $Si_{1-x}Ge_{x}$, $Si_{x}N_{y}$, or $Si_{x}ON_{y}$.

[c29] A semiconductor structure according to claim 26, wherein:the gate is an n-channel field effect transistor gate or a p-channel field effect transistor gate; and the stress imposing material is a material that introduces a tensile stress in a direction parallel to a direction of current flow if the gate is an n-channel field effect transistor gate, or a material that introduces a compressive stress in a direction parallel to a direction of current flow if the gate is a p-channel field effect transistor gate.

[c30] A semiconductor structure according to claim 26, wherein:the stress imposing material is a material that introduces a stress that enhances or degrades electron or hole mobility in the semiconductor structure.